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Estimation of the capacitor voltages in flying capacitor multi-level converters

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Abstract

Flying capacitor multi-level converters use charged capacitors as a critical element. For proper operation, the capacitor voltages must be known and regulated. Direct measurement is straightforward, but when the number of required measurements is high, this is a complicated approach. This paper introduces an estimation method for n capacitor voltages. The scheme is based on a system of $(n + 1)$ equations, which is defined in a way that it incorporates information of the actual capacitor voltages and open-loop estimates of the capacitor voltages. The solution of the system gives the best estimates of the capacitor voltages in the sense of least square errors. The method requires only output voltage and output current sensors and its computational burden is low, saving cost and design efforts, and simplifying the hardware system. The performance of the proposed scheme is evaluated experimentally in a 9-level flying capacitor chopper, where the estimates are used by the voltage balancing strategy and by the output current controller.

1 | INTRODUCTION

Multi-level converters were introduced with the invention of the neutral-point-clamped (NPC) converter [1]. Later, other multi-level topologies, as the flying capacitor multi-level converter (FCMC) [2], the cascaded H-bridge multi-level converter (CHBMC) [3], and the modular multi-level converter (MMC) [4], were developed. In one hand, multi-level converters allow using power electronics semiconductors in voltage levels higher than the blocking voltage of the individual power semiconductors, enabling the use of power electronics in middle and high voltage applications. Moreover, its output voltage is composed of more than two discrete voltage levels, improving its quality. On the other hand, each specific multi-level topology has a particular structure, but share a basic operating principle. In this sense, multi-level converters use a set of voltage sources which are series-connected by power semiconductors to get the multi-level output voltage waveform. There are several ways in which the voltage sources and power semi-conductors can be arranged, given raise to the known multi-level topologies [1–4]. In general, charged capacitors define the voltage sources in multi-level converters, which needs a control loop to ensure the required voltage level at each capacitor. Furthermore, each topology has specific requirements concerning the capacitor voltages which are needed to get a proper and safe converter operation. When the number of capacitors is high, maintaining the required voltage level at each capacitor is a challenging task.

Due to its high-quality waveforms and its capability to operate at higher voltages than individual semi-conductors, multi-level converters are attractive for applications in medium or high-voltage levels [5–8]. More recently, the FCMC is proposed for applications where high-density power and high-quality waveforms are required. In [9], an active power filter based on a 3-level 4-leg FCMC is proposed, and in [10] a flying-capacitor (FC) bridge is incorporated into a full-scale converter for direct-drive wind turbines. Also, in [11] an FC-MMC is presented for medium-voltage motor drives, and in [12] an FC fly back converter for pulsed power applications is proposed. Furthermore, 7-level FCMC are applied to single-phase inverters in [13] and as a power factor correction front end boost converter in [14]. Also, in [15] a single-phase N-level FC multi-level rectifier is used in a solid-state transformer, and a compact dual-output inverter is presented in [16]. Finally, in [17] a 9-level FCMC for electric aircraft applications is proposed and a 13-level inverter is presented in [18]. These applications

demonstrate the potential of the FCMC using a high number of levels, where the property of natural balance is used to achieve the required voltage at each capacitor. Several works have studied this property, and proposed techniques to improve its dynamics, especially at start-up when the input dc voltage increases from zero to nominal value [19–22]. Furthermore, closed-loop strategies are used to improve the capacitor voltage balancing dynamics [23–28]. Indeed, the closed-loop control of the capacitor voltages is an area actively researched. Most of the proposed techniques require to know the capacitor voltages to implement a closed-loop control strategy. Direct measurement is straightforward, but when the number of capacitors is high, direct measurement becomes a complicated task. In this case, it is more convenient to use a reduced number of sensors, and indirectly measure the voltages using estimation or observation techniques. In this sense, there are several proposals to simplify the capacitor voltage measurement task [29]-[41]. Estimation and observation techniques are based on measurements of the output current or the output voltage or both, which combined with the system model allow to know the capacitor voltages using a reduced number of sensors. Some proposed techniques are based on non-linear theory [29–31] or sliding mode approaches [32, 33]. These approaches have fast response, and good performance under parameter uncertainty, but its complexity restraint their real-time implementation, and tuning the observer gains is difficult, especially when they are implemented in discrete time with relatively big sample times. In [33], a discrete sliding mode observer is proposed, and some guidelines are given to select the gains. Other proposals use the output voltage measurement to measure the capacitor voltages indirectly. Indeed, there exist some switching states where only one capacitor determines the output voltage; in this case, the voltage of that capacitor is equal to the measured output voltage. In [34], this is applied to an MMC, using a single voltage sensor for a subset of modules. Whenever only one of these modules is active, then its voltage is equal to the measured output voltage. If more than one module is active, then the voltages are estimated using an open-loop approach. The error introduced by the open-loop estimation is corrected by enforcing a measure sequence at predefined times, which introduces additional complexity to the scheme. A similar approach is used in [35] with a flying capacitor converter. Here, the estimation scheme is presented using the formalism of Petri nets. Furthermore, [36] propose to divide the modules in an MMC into several groups and use one voltage sensor for each group. Several cases are considered to estimate the voltage of each group accurately. In these schemes, correction of the open-loop induced errors needs the introduction of a particular measuring sequence, which adds complexity to the system.

Other estimation schemes are based on linear quadratic schemes [37–40]. Since the output voltage is a linear combination of the capacitor voltages, then several consecutive measurements are expressed as a system of linear equations — the solution of this system gives an estimate of the capacitor voltages. In [37], the capacitor voltages in an FCMC are estimated using this principle. An over-determined system of equations is defined from consecutive output voltage measurements, and then solved to find an estimate of the capacitor voltages, however, a unique solution is not always possible. Moreover, this approach needs a high sampling rate, putting restrictions for its real-time implementation. In [38], an adaptive linear neuron and a recursive least-squares algorithm are proposed. Both algorithms are similar in the sense that both need a design parameter for the correction term, but the recursive least-squares needs a higher number of calculations. Another linear quadratic estimation scheme is proposed in [39] to estimate the state variables in an MMC. Also, in [40], the Kalman filter is used in an MMC, where a linear combination of the capacitor voltages models the output voltage, and the Kalman filter is used to estimate the capacitor voltages from the output voltage measurements. Also, an open-loop predictor combined with a simplified version of the Kalman filter is proposed in [41]. Here, the open-loop prediction of the output voltage is compared with its measurement to introduce a correction term in the open-open loop estimation. The scheme is applied to an MMC and verified by numerical simulations.

In this paper, we propose a simple and efficient estimation scheme for the n voltages of the FCMC. The scheme is based on a system of $(n+1)$ equations requiring only output voltage and current sensors, saving cost and design efforts, and simplifying the hardware system. The first equation models the output voltage as a linear combination of the capacitor and input voltages, the other n equations contain the information of previous estimates. The solution of the system, in the sense of least-square-errors, gives the best estimate of the capacitor voltages, at each sampling time. Among its distinctive features, we have its straightforward implementation, its low computational burden, good precision, and the absence of adjustment parameters. Moreover, the scheme can be applied to converters with an arbitrary number of voltage levels. Furthermore, the scheme is validated by simulation and experimentally in a 9-level flying capacitor chopper, where the estimated voltages are used to implement a closed-loop control strategy for the capacitor voltages and output current.

The rest of the paper is organised as follows. In Section 2, the general model of a multi-level converter is developed. After developing the model, the estimation scheme is introduced in Section 3, and its application to a 9-level flying capacitor chopper is presented in Section 4. Then in Section 5, the test bench is described and simulation results are presented in Section 6. The experimental results are analysed in Section 7, and the conclusions outlined in Section 8.

2 | MULTI-LEVEL CONVERTERS

Multi-level converters can be represented by the serial connection of controlled voltage sources, as shown in Figure 1, where in most cases, charged capacitors are used instead of voltage sources. The control input of the jth voltage source is a discrete function, $\delta_j \in \{-1, 0, 1\}$. In this section, we develop a general model for a multi-level converter; the model is intended to develop the estimation scheme for the capacitor voltages.

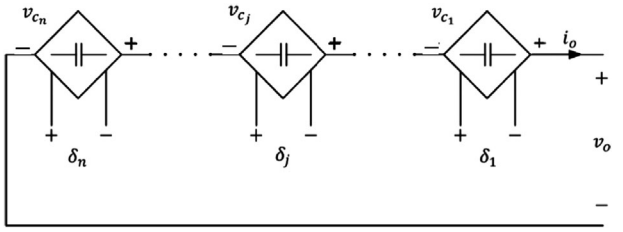

FIGURE 1 Equivalent circuit of a generic multi-level converter

2.1 | Multi-level converter model

Figure 1 shows an equivalent circuit of a multi-level converter, modelled as the serial connection of controlled voltage sources. From Figure 1, the output voltage is defined by a linear combination of the n voltage sources, expressed as

$$v_o(t) = \sum_{j=1}^{n} \delta_j(t) \cdot v_{c_j}(t) \tag{1}$$

where $\delta_j(t)$ and $v_{c_j}(t)$ are the commutation function and the voltage of the jth voltage source, respectively. The commutation function $\delta_j(t)$ is defined by the control signals of the power semiconductors.

When capacitors are used to define the voltage sources, their voltage dynamics is given by

$$v_{c_j}(t) = v_{c_j}(0) + \frac{1}{C_j}\int_0^t i_{c_j}(t) \cdot dt \tag{2}$$

where $v_{c_j}(0)$, $i_{c_j}(t)$ and C_j are the initial voltage, the current and the capacitance of the jth capacitor, respectively. In this model we assume that the equivalent series resistance (ESR) of the capacitors is negligible. The current through the jth capacitor is defined by the output current and the commutation function as

$$i_{c_j}(t) = -\delta_j(t) \cdot i_o(t) \tag{3}$$

where $i_o(t)$ is the converter output current.

2.2 | Discrete model

Let us suppose that the converter variables are known only at discrete instant times $t = k\Delta t$, where $k \in \mathbb{N}$ and Δt is the time elapsed in between sampling instants. Then, at time k, the output voltage is given by

$$v_o^k = \sum_{j=1}^{n} \delta_j^k \cdot v_{c_j}^k \tag{4}$$

where $(\cdot)^k$ are variables defined at instant time k.

Furthermore, the capacitor voltages are given by

$$v_{c_j}^k = v_{c_j}^{k-1} + \frac{i_c^k}{C_j} \cdot \Delta t \tag{5}$$

where we assume that Δt is small, such that $i_{c_j}^k \approx i_{c_j}^{k-1}$. Then, introducing Equation (3) into Equation (5), the capacitor voltages are expressed as

$$v_{c_j}^k = v_{c_j}^{k-1} - \delta_j^k \frac{i_o^k}{C_j} \cdot \Delta t. \tag{6}$$

Equations (4) and (6) are the basis for the estimation scheme that is introduced in Section 3.

3 | ESTIMATION OF THE CAPACITOR VOLTAGES

Let us assume that at time k the output current and output voltage are measured, the commutation functions are known, and an estimate of the capacitor voltages at time k-1 is available. Then, from Equation (6), the *a priori* (or open-loop) estimation of the capacitor voltages, at time k, is given by

$$\hat{v}_{c_j}^{k-} = \hat{v}_{c_j}^{k-1} - \delta_j^k \frac{i_o^k}{C_j} \cdot \Delta t \tag{7}$$

where $\hat{(\cdot)}^{k-}$ is the *a priori* or open-loop estimate at time k for the variable $(\cdot)$.

On the one hand, Equation (7) gives estimate of the capacitor voltages that are subject to the well-known limitations of open-loop estimators; on the other hand, the measurement of v_o^k is a linear combination of the actual capacitor voltages at time k. Then, the open-loop estimates and the output voltage measurement can be used to form the following system of equations:

$$\underbrace{\begin{bmatrix} v_0^k \\ \hat{v}_{c1}^{k-} \\ \vdots \\ \vdots \\ \hat{v}_{cn}^{k-} \end{bmatrix}}_{\mathbf{V}_o^k} = \underbrace{\begin{bmatrix} \delta_1^k & \delta_2^k & \cdots & \delta_n^k \\ 1 & 0 & \cdots & 0 \\ 0 & 1 & 0 & \vdots \\ \vdots & 0 & \ddots & 0 \\ 0 & 0 & \cdots & 1 \end{bmatrix}}_{\mathbf{\Delta}^k} \underbrace{\begin{bmatrix} v_{c1} \\ v_{c2} \\ \vdots \\ v_{cn} \end{bmatrix}}_{\mathbf{V}_c^k} \tag{8}$$

where $\mathbf{V}_o^k \in \mathbb{R}^{(n+1)}$, $\mathbf{\Delta}^k \in \mathbb{Z}^{(n+1)\times n}$ and $\mathbf{V}_c^k \in \mathbb{R}^n$.

The over-determined system (8) can be solved to find the best estimates of the capacitor voltages in the sense of least-squares errors (LSE) at time k. The (pseudo-) solution to system (8) is given by

$$\hat{\boldsymbol{V}}_c^k = (\mathbf{\Delta}^{k^T}\mathbf{\Delta}^k)^{-1} \cdot \mathbf{\Delta}^{k^T} \cdot \mathbf{V}_o^k \tag{9}$$

where $\mathbf{\Delta}^{k^T}$ is the transpose matrix of the design matrix $\mathbf{\Delta}^k$, $(\mathbf{\Delta}^{k^T}\mathbf{\Delta}^k)^{-1}$ is the inverse matrix of $(\mathbf{\Delta}^{k^T}\mathbf{\Delta}^k)$ which is a square $(n \times n)$ matrix called the pseudo-inverse of $\mathbf{\Delta}^k$; the (pseudo-) solution of (9) is unique if $rank(\mathbf{\Delta}^k) = n$ which is always assured

by the last n rows of $\mathbf{\Delta}^k$. Indeed, $\hat{V}_c^k$ represents the best estimation of the capacitor voltages at time k, in the sense of LSE. These estimates are obtained by combining a measurement of the output voltage (a linear combination of the actual capacitor voltages), and the open-loop estimates of the capacitor voltages. Note that the introduction of the output voltage measurement allows adding a closed-loop correction term to the open-loop estimates.

3.1 | Estimation algorithm

Given the sparsity of matrix $\mathbf{\Delta}^k$, system (9) can be solved to find an explicit equation for each estimate. Solving Equation (9), each estimate is given by

$$\hat{v}_{c_j}^k = \hat{v}_{c_j}^{k-} + K_j^k \cdot (v_o^k - \hat{v}_o^{k-}) \tag{10}$$

where $\hat{v}_{c_j}^k$ is the estimate of the jth capacitor voltage, with $j = 1, \dots, n$; $v_{c_j}^{k-}$ is the *a priori* (or open-loop) estimate of the jth capacitor voltage, as defined by Equation (7); v_o^k is the measured output voltage, and $\hat{v}_o^{k-}$ is the *a priori* estimation of the output voltage, given by

$$\hat{v}_o^{k-} = \sum_{j=1}^{n} \delta_j^k \cdot \hat{v}_{c_j}^{k-} \tag{11}$$

the gain K_j^k is defined as

$$K_j^k = \frac{\delta_j}{1 + \sum_{j=1}^{n} \delta_j^2}. \tag{12}$$

Thus, the proposed estimation scheme is defined by Equations (7), (10), (11) and (12), where Equation (10) is the explicit equation for each estimate, Equation (7) represents the *a priori* estimates of the capacitor voltages, Equation (11) gives the *a priori* estimate of the output voltage and Equation (12) represents the gain for the correction term. Indeed , the output voltage measurement allows to add a correction term based on the actual capacitor voltages which improves the open-loop estimates.

4 | ESTIMATION OF THE CAPACITOR VOLTAGES IN A FLYING CAPACITOR MULTI-LEVEL CONVERTER

In this section, we apply the estimation algorithm to FCMC, which equivalent circuit is shown in Figure 2. It consists of n voltage sources, that can be connected in series by the action of the switches control signals, d_j and $\tilde{d}_j$. Proper operation of the converter requires complementary control signals, d_j and $\tilde{d}_j$ [2].

Let define the control signal applied to the upper switch of cell j as $d_j \in \{0, 1\}$, where 0 and 1 define the *off* and *on* state,

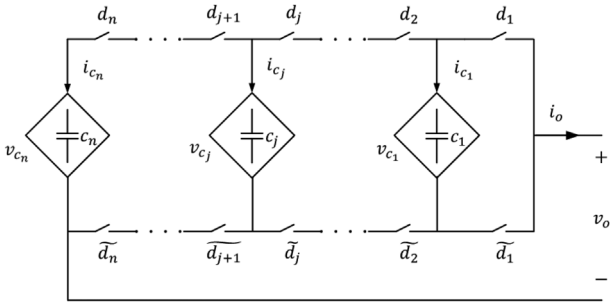

FIGURE 2 Equivalent circuit of a FCMC

respectively. Then at time k, the following commutation function is defined

$$\delta_j^k = d_j^k - d_{j+1}^k \qquad j = 1, \dots, n \qquad d_{n+1} = 0 \tag{13}$$

where $\delta_j^k \in \{-1, 0, 1\}$. Furthermore, the output voltage is defined as a linear combination of n voltage sources, as

$$v_o^k = \sum_{j=1}^{n} \delta_j^k \cdot v_{c_j}^k \tag{14}$$

where $v_{c_j}^k$, from $j = 1, \dots, n-1$, and $v_{c_n}^k$ are the flying capacitor voltages and the input voltage at time k, respectively.

Moreover, the capacitor voltages are given by

$$v_{c_j}^k = v_{c_j}^{k-1} - \delta_j^k \frac{i_o^k}{C_j} \cdot \Delta t. \tag{15}$$

Equation (15), for $j = 1, \dots, n-1$, represents the flying capacitor voltages, and for $j = n$ it represents the input voltage source; if the input voltage is considered constant between sampling times, then the second term in the right hand side of Equation (15) is equal to zero for $j = n$. Moreover, the following voltage values at each capacitor are needed:

$$v_{c_j}^* = \frac{V_{DC}}{n} j \qquad j = 1, \dots, (n-1) \tag{16}$$

where $v_{c_j}^*$, n and V_{DC} are the voltage reference for the jth capacitor, the number of commutation cells and the input voltage, respectively. These capacitor voltages are necessary to distribute the input voltage between the series-connected switches evenly, and also to obtain an output voltage composed of discrete voltage levels of equal magnitude. Indeed, these capacitor voltages are a necessary condition for the proper and safe converter operation [2]. Equations (14) and (15) are identical to Equations (4) and (6) of the generic converter described in Section 2, and therefore, the estimation of the capacitor voltages can be achieved applying the method presented in Section 3. Thus, the estimation of the capacitor voltages is given by Equations (7), (10), (11) and (12), where the commutation functions are defined by Equation(13).

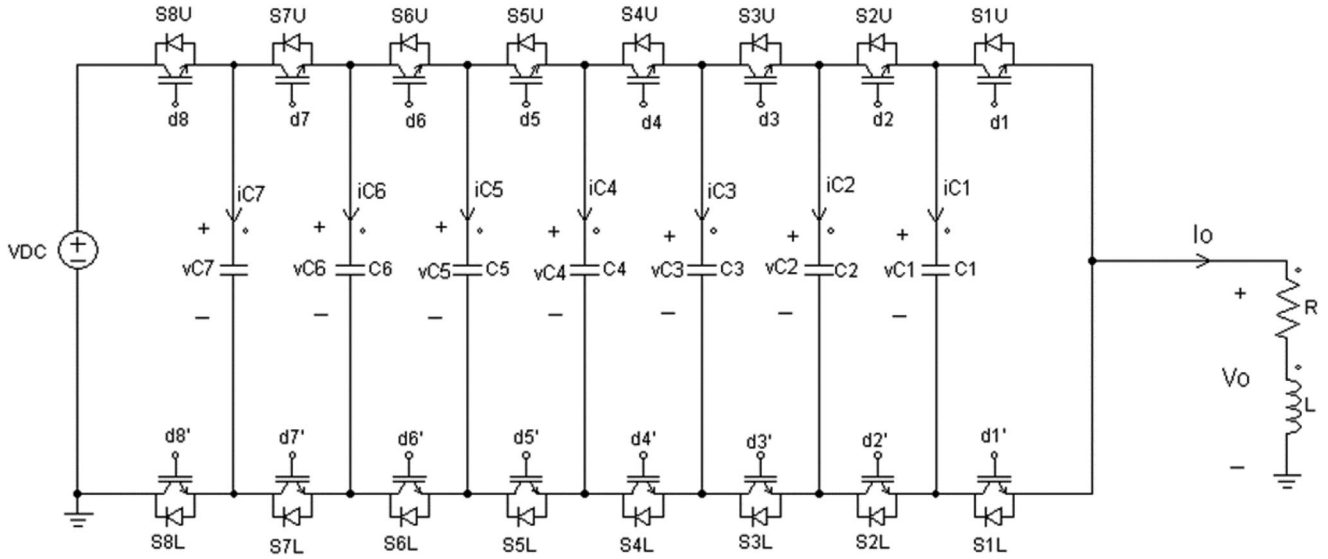

FIGURE 3 9-level FCMC with R-L load

5 | TEST BENCH

In this section, we explain how the proposed estimation algorithm is used in a 9-level FCMC system. Figure 3 shows a 9-level FCMC, which is composed of eight commutation cells. Each commutation cell is defined by a pair of complementary switches (SjU and SjL) and capacitor C_j, where $j = 1, \dots, 8$; note that for j=8 that capacitor defines the input voltage V_{DC}. The cell switches are controlled by complementary control signals dj, dj', where $j = 1, \dots, 8$. The complete system includes the control strategy for the capacitor voltages balance and the output current controller, as shown in Figure 4. The test bench is composed of a 9-level FCMC configured as a chopper with and R-L load. The estimation and control algorithms are periodically executed on a dSPACE 1104 control board, with a sampling period $T_s = 75\mu s$. First, the estimation algorithm estimates the capacitor voltages using the methodology explained in Sections 3.1 and 4. Next, the output current controller calculates the output voltage level to regulate the output current. The current controller is based on a finite control set model predictive controller (FCS-MPC) [35]. To find the voltage level needed for the output current regulation, we calculate, one step ahead, the output current, considering each available voltage level, as follows:

$$i_j^{k+1} = \left(i_o^k - \frac{v_{x_j}}{R}\right) e^{-\frac{T_s}{\tau}} + \frac{v_{x_j}}{R} \qquad for \qquad j = 0, 1, \dots, n \tag{17}$$

where v_{x_j} are the available voltages, defined as

$$v_{x_j} = j\frac{\hat{V}_{DC}}{n} \qquad for \qquad j = 0, 1, \dots, n \tag{18}$$

and $\hat{V}_{DC}$ is the estimated input voltage; T_s is the sampling period and $\tau = L/R$ is the load constant time. Then, a cost function, $J(i_j)$, is defined as the absolute value of the predicted output current error for each available voltage level

$$J(i_j) = |i_j^{k+1} - i_o^{*(k+1)}| \qquad for \qquad j = 0, 1, \dots, n \tag{19}$$

where $i_o^{*(k+1)}$ is the reference current. The voltage level that minimises Equation (19), is selected as the required voltage level v_x^*.

Finally, the balancing strategy selects the switching state that balances the capacitor voltages and ensures the required voltage level, simultaneously. This strategy uses the capacitor and input voltages estimates to decide if the capacitor voltages must be increased or decreased, according to Equation (16). The capacitor voltage balancing strategy is based on the redundancy of switching states and directly provides the control signals for the FCMC [28]. Note that the switching frequency is variable, but the estimation process is executed periodically at a sampling frequency of $f_s = 1/T_s$. This simplifies the estimation process because for calculating the *a priori* capacitor voltages, using Equation (7), Δt is always equal to T_s. When modulation schemes are used, the switching frequency is constant; however, the duty cycle and the duration of the switching states are variable, which imposes some restrictions on the estimation scheme. In this case, it is necessary to use a sampling frequency much higher than the commutation frequency to prevent the loss of data when the duration of the switching states is small. However, for some duty cycles, there will be some switching states that can not be detected in detriment of the accuracy. Also, higher the sampling frequency, more computational power will be necessary to shorten the algorithm execution time.

It is worth to mention that with the used balancing strategy [28], the maximum voltage ripple in the capacitors is given by

$$\Delta V_{c_{Max}} = 2\frac{I_{o_{Max}}}{C} T_s \tag{20}$$

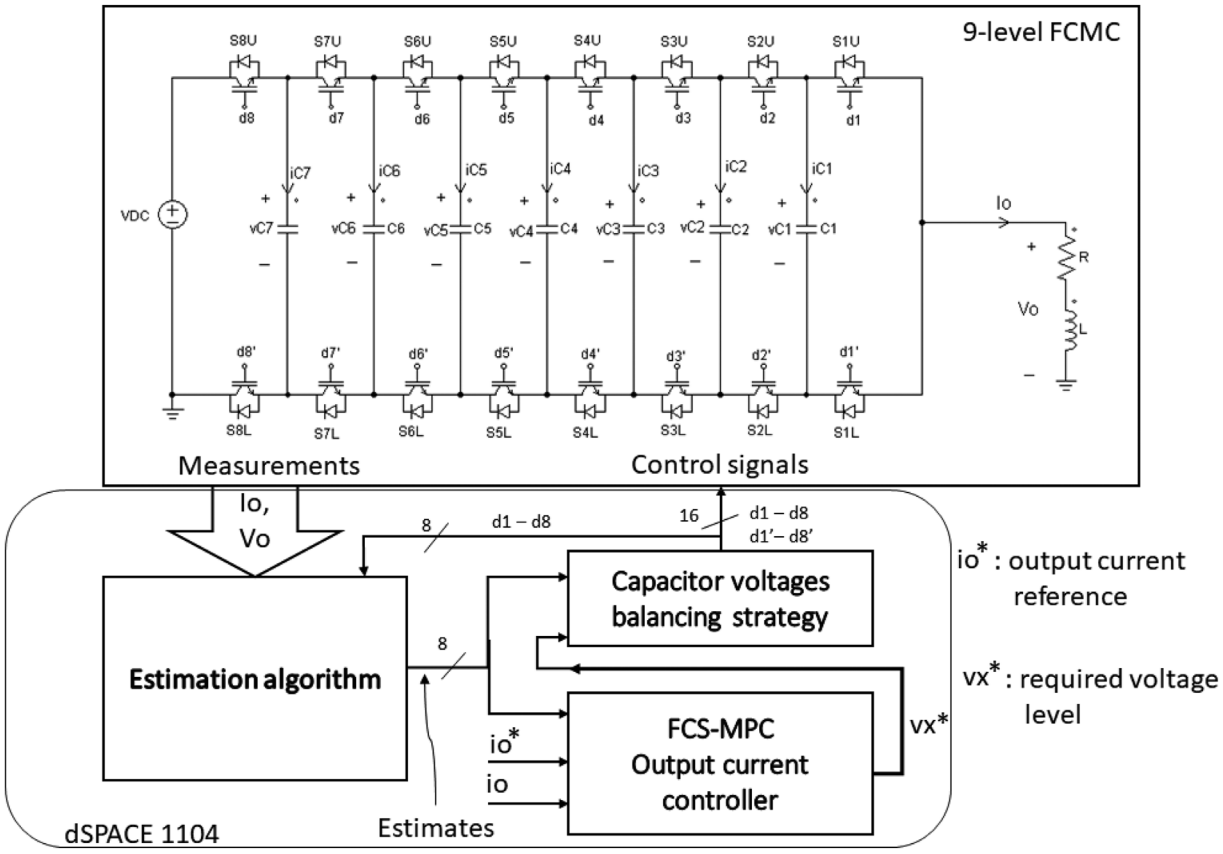

FIGURE 4 Block diagram of the test bench system

TABLE 1 Nominal parameters of test bench system

Parameter	Value
Number of commutation cells, n	8
Flying capacitance, C	390 μF
C nominal equivalent series resistance, ESR	2.4 $m\Omega$
Load resistance, R	12.6 Ω
Load inductance, L	3.6 mH
Input voltage V_{DC}	100 V
Sampling period, Δt	75 μs

where $I_{o_{Max}}$, C and T_s are the maximum output current, the capacitance value and the sampling time, respectively.

6 | SIMULATION RESULTS

In this section, we present simulation results to evaluate the performance of the proposed estimation algorithm. The nominal parameters of the test bench system are given in Table 1.The software Matlab/Simulink is used to simulate the system, where the power converter simulation uses a time-step of $1\mu s$ and the estimation algorithm, output current controller and capacitor balancing strategy are executed sequentially each $75\mu s$. The reference current, i_o^*, is defined as a sinusoidal waveform with a dc offset

$$i_o^* = 4 + 3.5\sin(\omega t)A$$

where $\omega = 2\pi f$ with $f = 60Hz$. First, we show results using direct measurements of the capacitor and input voltages, assuming measurements without noise. Figure 5 shows the input voltage and capacitor voltages measurements. The capacitor voltages evolution is in a quasi-balanced manner as required for proper and safe converter operation. Figure 6 shows the output voltage and current and their respective total harmonic distortion (THD); also the current tracking error is shown, where we can observe that in steady-state it is about ± 0.1 A.

Next, we present results using the estimates instead of direct measurement of the voltages. Figure 7 shows the measured and estimated capacitor voltages and the estimation error. The capacitor voltages evolution is similar to the obtained with direct measurements (see Figure 5). The estimation error is less than 1V, even if at start-up, it reaches higher values than in steady-state. However, the capacitor voltages evolution is quasi-balanced, ensuring the overstress on switches is limited to safe values. Figure 8 shows the output voltage and current and its respective THD, which values are practically the same as those obtained with direct measurements. Regarding the current tracking error, shown in Figure 8(c), it remains the same as the obtained with direct measurements.

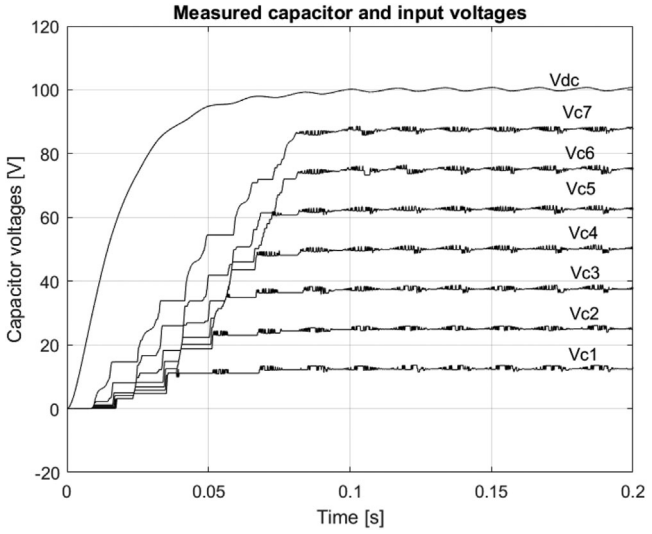

FIGURE 5 Simulation results using measured voltages: Measured capacitor and input voltages

However, in practice, the measured signals are corrupted by noise. To study the effect of noise in the system, we have added white noise to the output voltage and current measurements; the output voltage measurement noise has a maximum value of ±2V, while for the output current we considered a maximum noise value of ±100 mA.

Figures 9 and 10 show the effect of noisy measurements. We observe a quasi-balanced capacitor voltages evolution at start-up, and an estimation error in steady-state of about ±1.5 V – Note that the estimation errors are calculated using the measurement of the capacitor voltages without noise. Regarding the THD of the output voltage and current, it is 16.52% and 2.46%, respectively, and the output current tracking error is about ±0.15A.

Table 2 summarises the obtained results, where we have added an ideal case (first row), where constant voltage sources replace the capacitors; the voltage sources values are given by Equation (16). Also, results with an equivalent series resistance (ESR) of 10 times the nominal value are shown in the last row.

7 | EXPERIMENTAL RESULTS AND DISCUSSION

In this section, we present the results obtained in a 9-level flying capacitor chopper. Figure 4 shows the block diagram of the experimental test system and Fig. 11 shows the 9-level FCMC laboratory prototype. The experimental system consists of a 9-level flying capacitor converter, a variable *dc* voltage source, voltage and current transducers, a function generator and a dSPACE 1104 control board. The nominal parameters of the experimental system are given in Table 1. For the experimental test, we use an amplitude modulated dc biased sinusoidal at 60 Hz. The reason behind this choice is to test the estimation algorithm with a variable output current, which at some intervals will need only a reduced number of voltage levels.

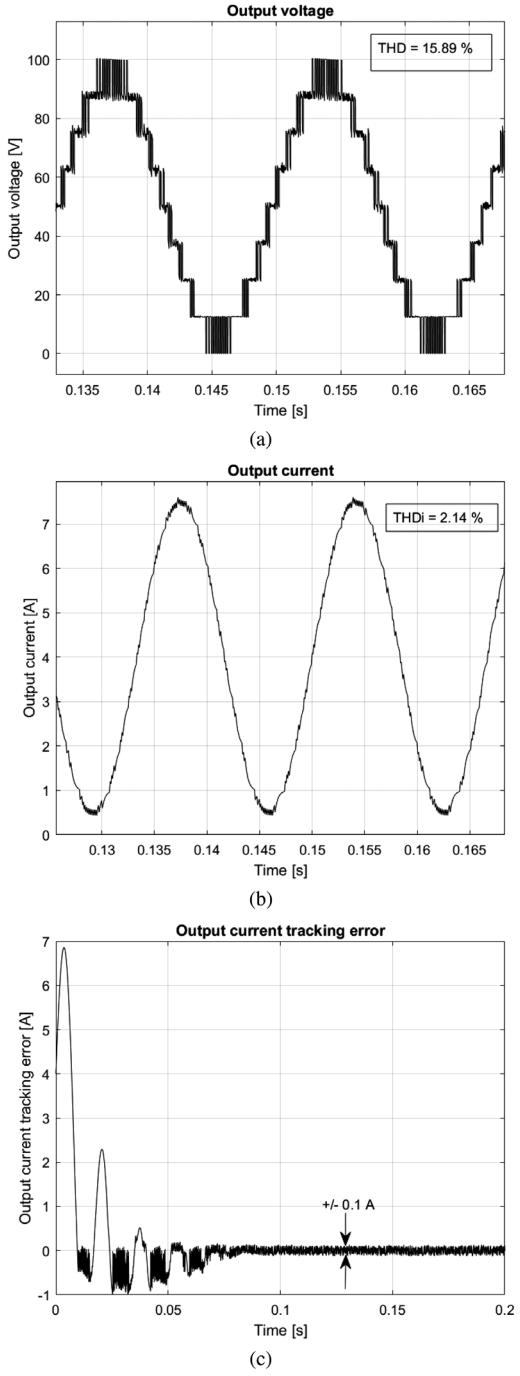

FIGURE 6 Simulation results using measured voltages. (a) Output voltage. (b) Output current. (c) Output current tracking error

The *dc* voltage source is connected to the converter input; the function generator provides the output current reference; the control board (dSPACE 1104) receives measurements of the output voltage and current, and executes the estimation and control algorithms each 75 μs. First, the capacitor voltages are estimated, then, the output current regulation loop calculates the required voltage level and finally, the capacitor voltages balance algorithm takes place, generating the control signals for the converter switches.

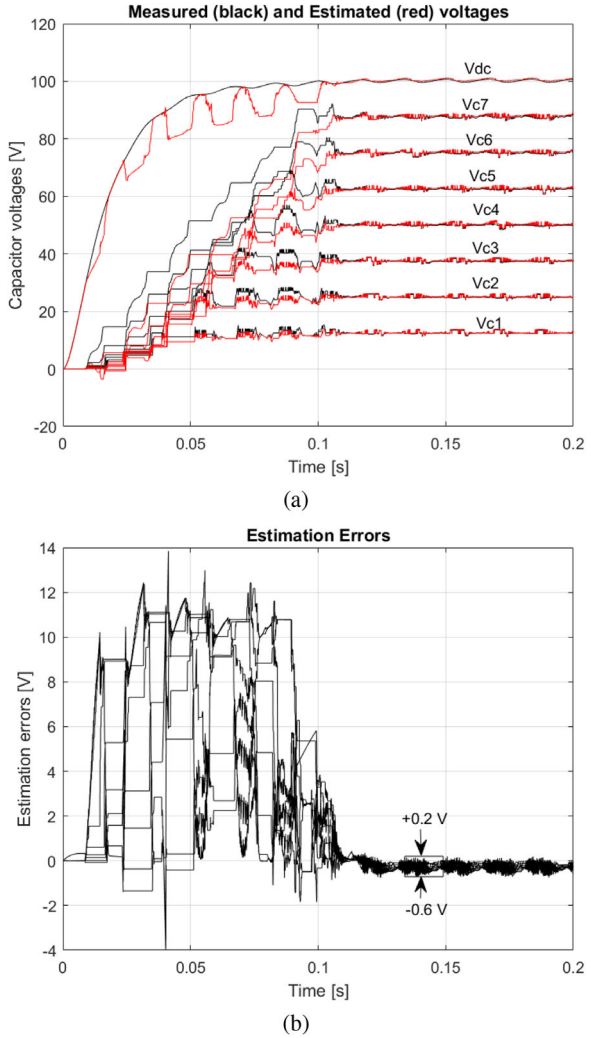

FIGURE 7 Simulation results using estimated voltages. (a) Measured (black) and estimated (red) capacitor voltages. (b) Estimation errors

7.1 | Steady-state performance

In this test, we evaluate the performance of the estimation scheme in steady-state. For that purpose, we compare the measured capacitor voltages with the estimated voltages. Note that the measured values are corrupted by noise, with maximum values of about ±2.0 V. Furthermore, we investigate the performance of the capacitors balance algorithm, which uses the estimates of the capacitor voltages. The capacitor voltage references are given by (16), where in the test bench V_{DC} is replaced by its estimate, $\hat{V}_{DC}$, resulting in

$$v_{c_j}^{*} = \frac{\hat{V}_{DC}}{n} j \qquad j = 1, \ldots, (n-1). \tag{21}$$

If the capacitor voltages are in accordance with Equation (21), the *off-state* switch voltages are given by

$$v_{sw} = \frac{V_{dc}}{n} \tag{22}$$

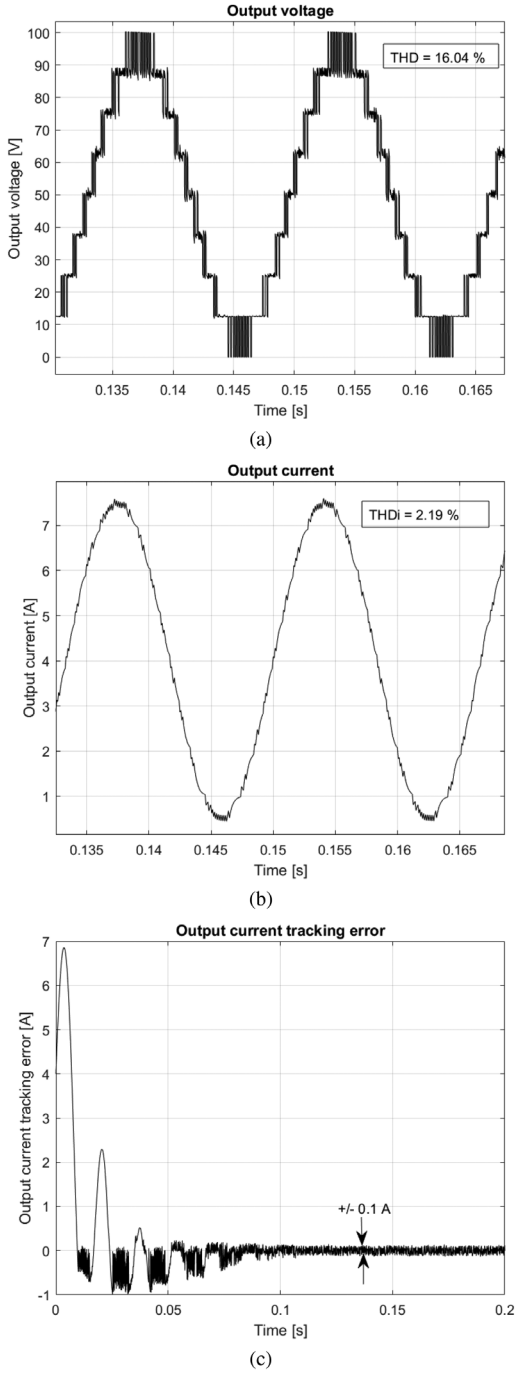

FIGURE 8 Simulation results using estimated voltages. (a) Output voltage. (b) Output current. (c) Output current tracking error

and the output voltage is composed of discrete voltage levels, where the magnitude of each discrete voltage levels is given by

$$v_{discr} = \frac{V_{dc}}{n}. \tag{23}$$

Figure 12 shows the converter output variables (top) and its zoomed view (bottom). The upper trace shows the output voltage, which is composed of equal magnitude discrete voltage levels. In one hand, this is possible only if the capacitor

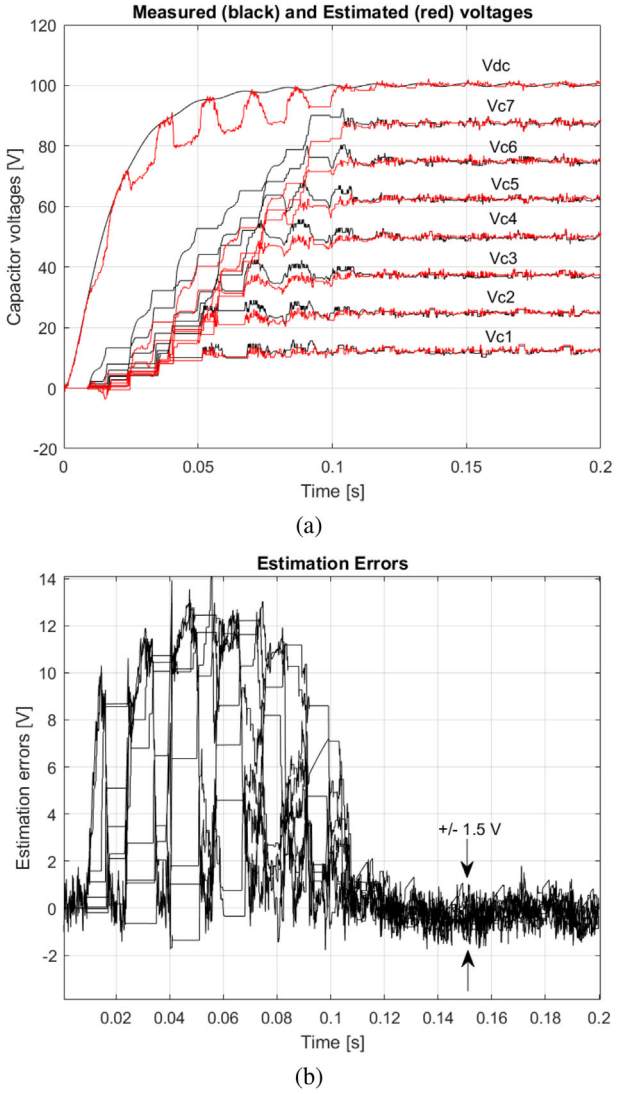

FIGURE 9 Simulation results using noisy measurements. (a) Measured (black) and estimated (red) capacitor voltages. (b) Estimation errors

TABLE 2 Performance indexes for different test conditions

Test condition	THD_V [%]	THD_i [%]	e_{v_c} [V]	e_i [A]
Ideal case	15.9	2.1	–	±0.1
w/Measurements	15.9	2.1	0.2	±0.1
w/Estimates	16.0	2.2	0.2	±0.1
Noisy measurements	16.5	2.5	1.5	±0.2
10X ESR	16.6	2.5	1.5	±0.2

THD_v Output voltage $THDTHD_i$Output current $THDe_{v_c}$Capacitor voltages estimation error e_iOutput current tracking error

voltages are correctly balanced, as defined in Equation (21). On the other hand, the balance of the capacitor voltages is possible only if the capacitor voltages are accurately estimated. Additionally, the middle trace shows the output current, and the bottom trace shows the output current error. Note that the output current is an amplitude modulated waveform. This is intended

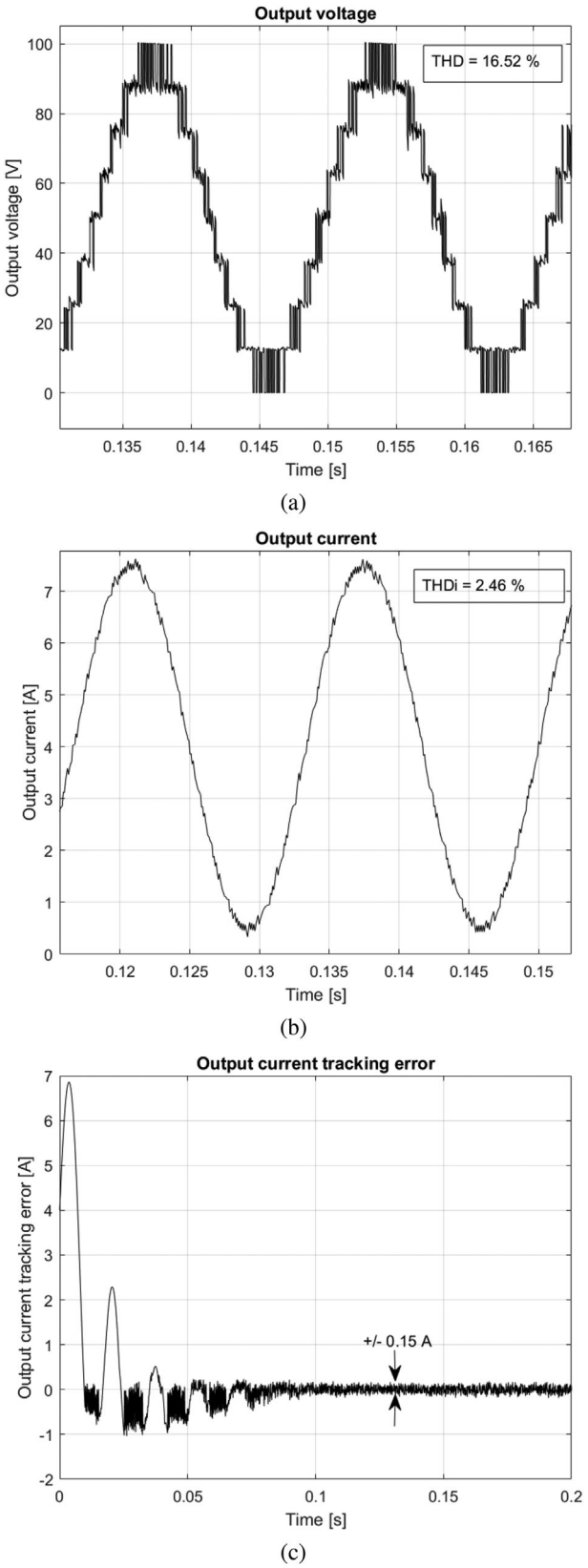

FIGURE 10 Simulation results using noisy measurements. (a) Output voltage. (b) Output current. (c) Output current tracking error

FIGURE 11 FCMC: 9-level laboratory prototype

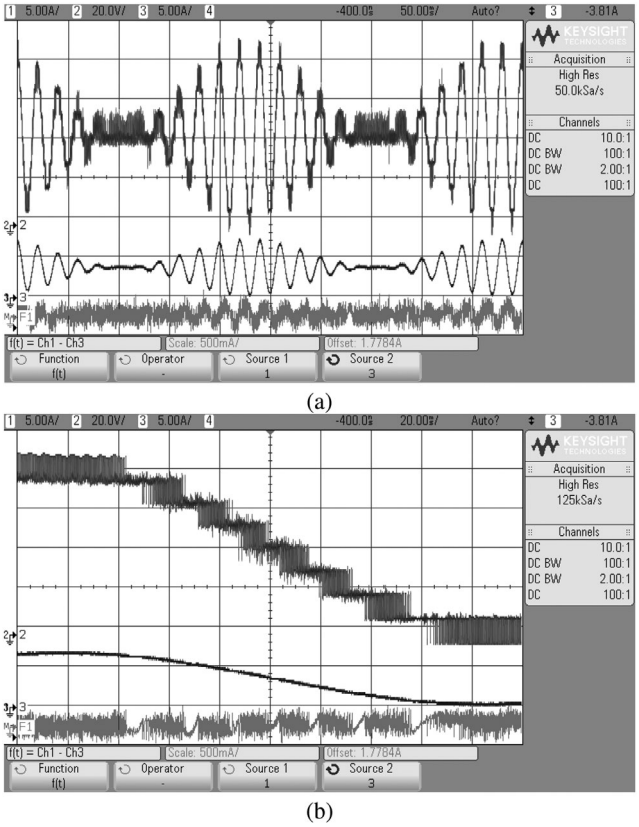

FIGURE 12 Converter output variables. (a) Normal view: (top trace) Output voltage 20 V/div, (middle trace) output current 5 A/div and (bottom trace) output current error 5 A/div. (b) Zoomed view

to test the estimation scheme with output voltages that contain all or only some of voltage levels. The output current error is bounded around $\pm 0.2A$, as observed in the bottom trace of Figure 12, indicating that the current control loop is also operating correctly. This initial test shows the excellent performance of the estimation scheme and demonstrates its potentiality in a real application.

Following, we show further results to evaluate the performance of the estimation scheme in steady-state. Figure 13 shows the estimated capacitor voltages and the estimation errors. As shown, the estimated and measured voltages are very close. Note that the measured and estimated values used to compute the errors have noise introduced by the measurement process, causing to observe a high-frequency component in the errors. Also, note that the input voltage has a low-frequency ripply, which is due to the output current variation. But its estimate is in concordance with the measured value. Furthermore, Table 3 shows the average voltage and maximum voltage ripple, $\Delta V_{c_{Max}}$, of the estimated and measured voltages; the theoretical maximum voltage ripple is given by Equation (20). As shown, the estimated and measured values are similar; the average values of the estimated and measured voltages are both in close concordance with the value defined in Equation (21), which confirms the good performance of the estimation scheme. Regarding the maximum observed voltage ripple, if we consider the noise introduced by the measuring process, it is also according to the theoretical value.

7.2 | Performance at start-up

In this test, we evaluate the performance of the estimation during the start-up process. During the start-up process, the input voltage, V_{DC}, changes from zero to its steady-state value. The main objective is to keep the *off-state* switch voltages at safe values, eliminating possible overstress on the semi-conductor switches. In this sense, the implemented closed-loop balancing strategy uses the estimated voltages to generate the control signals that ensure the balance of the capacitor voltages. Therefore, the estimation scheme must provide accurate estimates to keep the balance of the capacitor voltages, ensuring the safe operation of the converter switches during the start-up process.

Figure 14 shows the response of the system during the start-up process. The top window shows the estimated and measured capacitor voltages –when the input voltage starts to rise, the estimation errors are higher, but the capacitor voltages reach their desired equalised values in a quasi-balanced manner, at $t \approx 0.2s$– (see the middle window in Figure 14). The estimation error is higher when some of the capacitor voltages have the same value. Indeed, the converter model is valid only when $v_{c1} < v_{c2}, \ldots, < v_{cn}$. If this is not the case, the estimation scheme is not able to accurately estimate the capacitor voltages.

The bottom window of Figure 14 shows the *off-state* switch voltages. The voltage of the switches reaches its required value, as defined by Equation (22), at about 0.2 s. Note that in this test, no particular procedure has been considered in the closed-loop balancing strategy to start-up the converter. The same

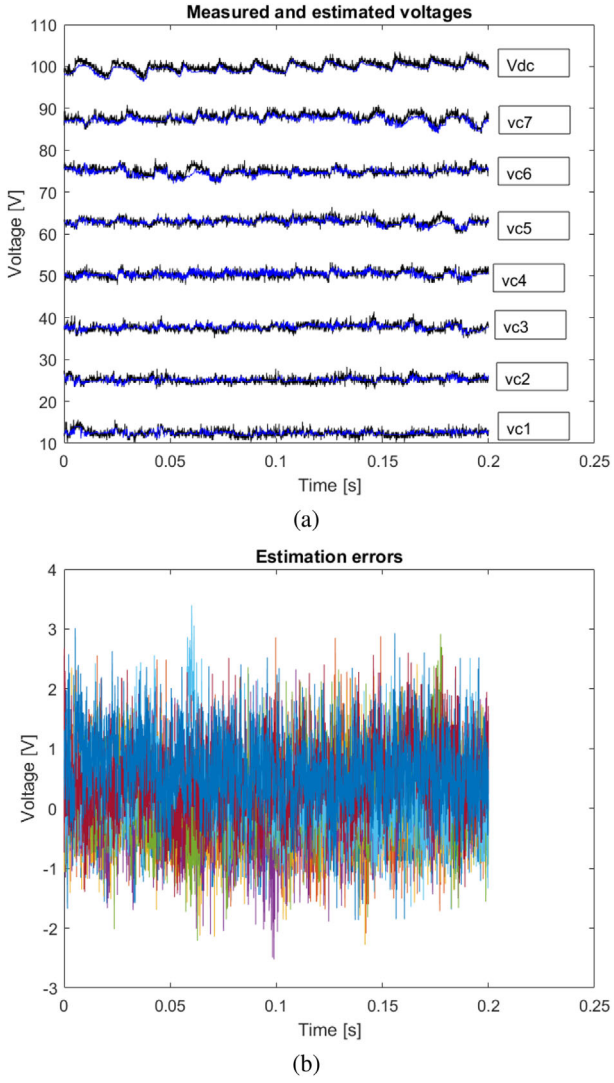

FIGURE 13 Steady-state performance. (a) Estimated (blue) and measured (black) capacitor voltages in steady-state. (b) Estimation errors

closed-loop balancing strategy operates during the start-up process and in steady state.

7.3 | Performance under an input voltage change

In this test, we evaluate the performance of the estimation scheme when the input voltage changes its value (it is increased or decreased) from a given steady-state value. In such events, the balance strategy, that uses the estimates of the capacitor voltages, must properly operate to prevent overstress of the converter switches. Especially during the voltage rise, the correct capacitor voltages balance ensures the *off-state* switch voltages at secure values. Also, if an external control loop uses the estimated voltages, then an accurate estimation is desired to minimise the effect of these transients on the external control loop.

Figure 15 shows the response of the system when the input voltage decreases from 100 V to 70 V, and then it returns to its

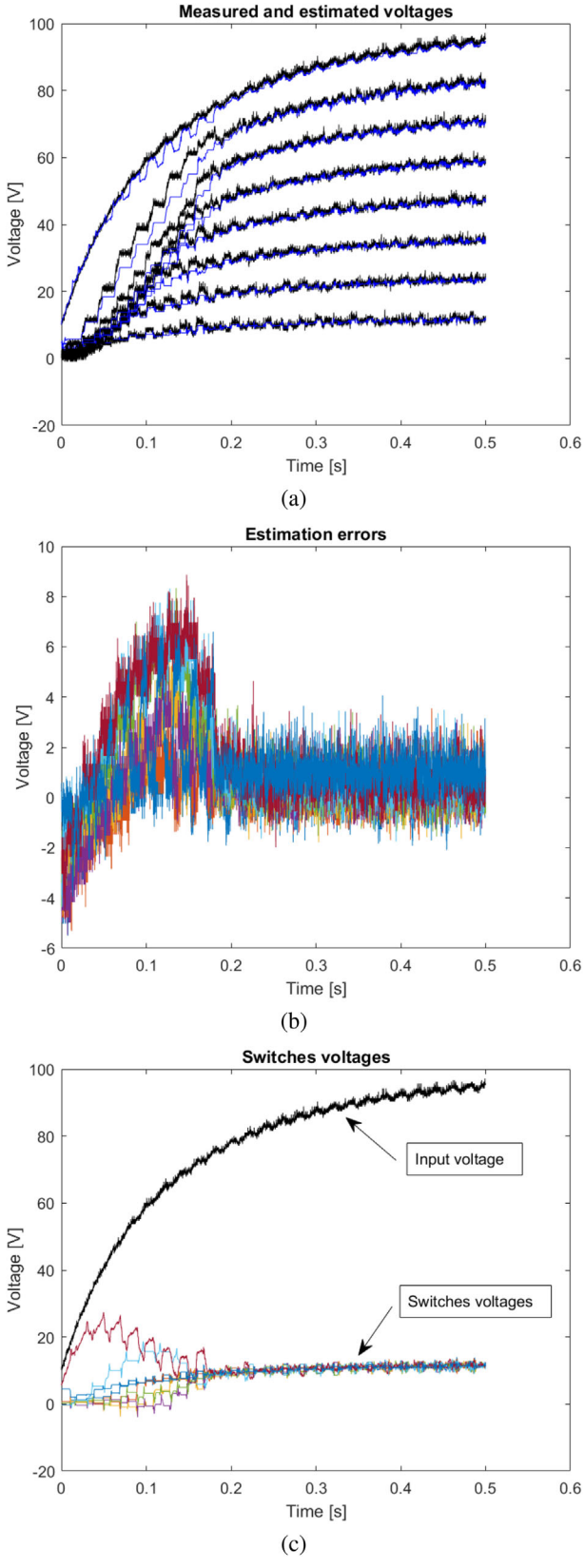

FIGURE 14 Performance at start-up. (a) Estimated (blue) and measured (black) capacitor voltages. (b) Estimation errors. (c) Input voltage and switch OFF voltages

TABLE 3 Estimated and measured voltages: Average voltage and maximum voltage ripple ($\Delta V_{c_{Max}}$) at each capacitor

Voltage	Average voltage [V]	$\Delta V_{c_{Max}}$ [V]
$\hat{v}_{c_1}$	12.4	2.8
v_{c_1}	12.5	5.3
$\hat{v}_{c_2}$	25.1	3.2
v_{c_2}	25.2	5.3
$\hat{v}_{c_3}$	37.7	3.6
v_{c_3}	37.7	6.3
$\hat{v}_{c_4}$	50.3	3.7
v_{c_4}	50.4	5.3
$\hat{v}_{c_5}$	62.9	4.2
v_{c_5}	63.0	6.3
$\hat{v}_{c_6}$	74.7	5.1
v_{c_6}	75.0	6.3
$\hat{v}_{c_7}$	87.4	5.4
v_{c_7}	87.8	6.8
$\hat{v}_{c_8}$	99.5	5.6
v_{c_8}	100.1	6.8

steady-state value of 100 V. At Figure 15(a), the input voltage, the estimation errors and the off-state switch voltages are shown at the top, middle and bottom traces, respectively. The estimation errors during the transients are similar to the steady-state errors, meaning that the estimation scheme can accurately estimate the voltages of the capacitors under this type of transients. We notice a small increase in the *off-state* voltage of the switches, which means that the capacitor voltages are slightly unbalanced. This unbalance happens because the output current during the transient has a small value. A small output current limits the voltage dynamics, preventing to accurately follow the input voltage dynamics according to Equation (21). Nevertheless, the accuracy of the capacitor voltages estimation is practically the same as in steady-state. Notice that unlike what happened in the start-up transient, in this case, the estimates of the capacitor voltages are accurate. This accuracy is possible because the voltages of the capacitors are such that $v_{c1} < v_{c2}, \ldots, < v_{cn}$, ensuring the validity of the used model.

Furthermore, Figure 15(b) shows the output current, which remains regulated as long as there is enough voltage for its control; otherwise, the control strategy will use the maximum available voltage to ensure the minimum possible error in the output current. These results confirm the excellent performance of the estimation scheme when a transient occurs in the input voltage.

7.4 | Performance with uncertain parameters

In this test, we evaluate the performance of the estimation scheme when the capacitance values are uncertain. Indeed, the actual capacitors in the laboratory prototype have nominal tolerance of ±10%.

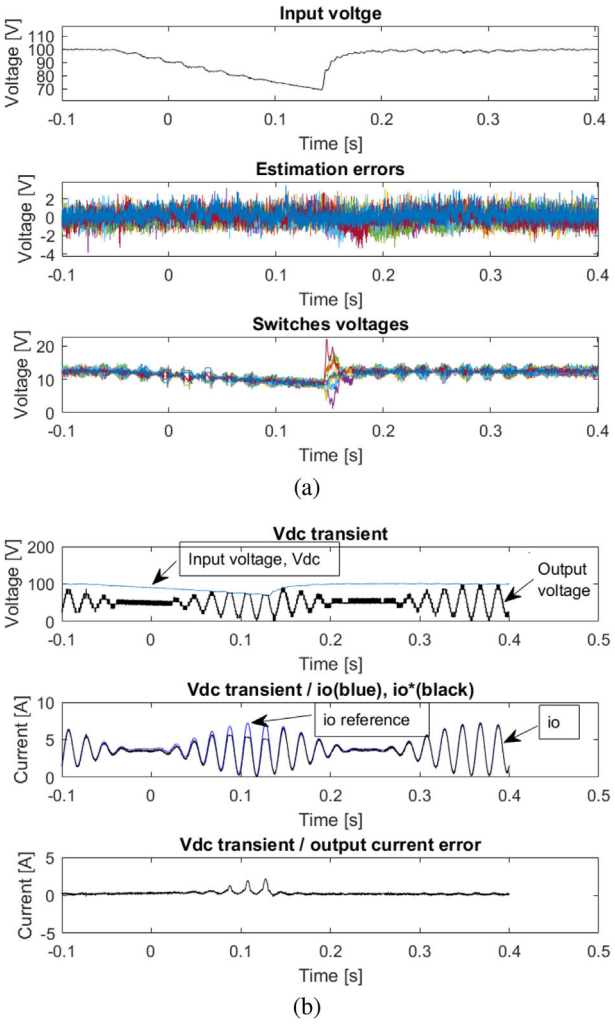

FIGURE 15 Performance under an input voltage change. (a) Top window: Input voltage; middle window: Capacitor voltage estimation errors; bottom window: Switch voltages. (b) Top window: Input and output voltages; middle window: Current reference (blue) and output current (black); Lower window: Output current error

In a first test, a capacitance of 300 μF is assumed, while the nominal value is 390 μF. Figure 16, shows the estimated capacitor voltages and the estimation errors, and Table 4 shows the average voltage and the maximum voltage ripple of each capacitor voltage. Both measured and estimated values are similar, which means that estimated values are as good as the measurements even if the assumed capacitance values are only 77% of the nominal values. The estimation errors are small, ensuring an accurate balance of the capacitor voltages, as shown in the top window of Figure 16. Moreover, data in Table 4 shows that the average capacitor voltages (measured values) are accurately regulated according to Equation (21).

In a second test, the capacitance values are 15% higher than the nominal values (i.e., $C = 1.15C_{nom} = 450\mu F$). Figure 17 shows the estimated capacitor voltages and the estimation errors, and Table 5 shows the average voltages and the maximum voltage ripple of the estimated and measured voltages. The mean values of the capacitor voltages are according to

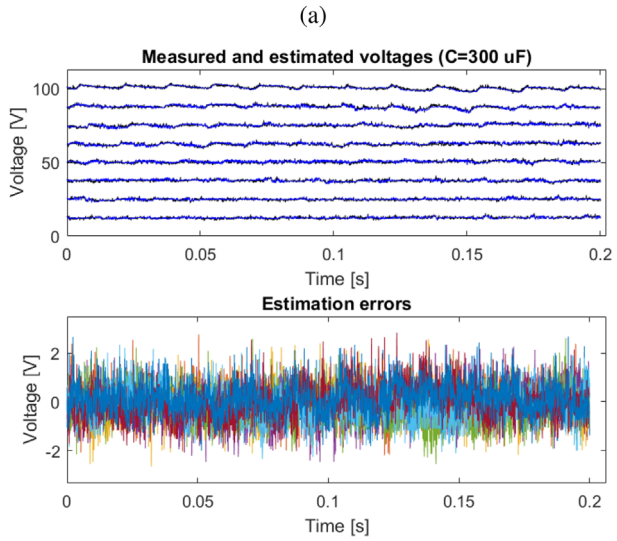

FIGURE 16 Uncertain capacitance, $C = 0.77C_{nom}$. (a) Measured (black) and estimated (blue) capacitor voltages. (b) Estimation errors

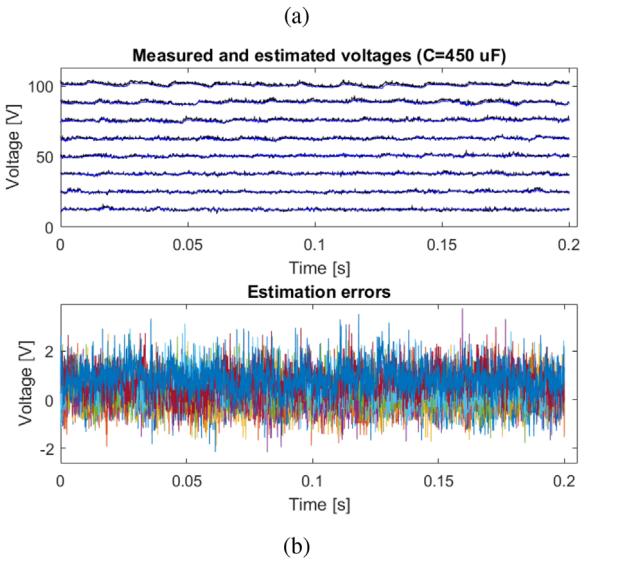

FIGURE 17 Uncertain capacitance, $C = 1.15C_{nom}$. (a) Measured (black) and estimated (blue) capacitor voltages. (b) Estimation errors

TABLE 4 Estimated and measured voltages with uncertain capacitance, $C = 0.77C_{nom}$: Average voltage and maximum voltage ripple ($\Delta V_{c_{Max}}$)

Voltage	Average voltage [V]	$\Delta V_{c_{Max}}$ [V]
$\hat{v}_{c_1}$	12.4	3.2
v_{c_1}	12.5	5.3
$\hat{v}_{c_2}$	25.1	4.1
v_{c_2}	25.0	5.8
$\hat{v}_{c_3}$	37.7	4.2
v_{c_3}	37.6	5.8
$\hat{v}_{c_4}$	50.5	4.4
v_{c_4}	50.4	5.8
$\hat{v}_{c_5}$	62.7	4.9
v_{c_5}	62.4	6.8
$\hat{v}_{c_6}$	75.4	5.4
v_{c_6}	75.2	6.3
$\hat{v}_{c_7}$	87.8	6.9
v_{c_7}	87.7	7.3
$\hat{v}_{c_8}$	100.7	5.6
v_{c_8}	100.8	7.8

TABLE 5 Measured and estimated capacitor voltages with uncertain capacitance, $C = 1.15C_{nom}$: Average voltage and maximum voltage ripple ($\Delta V_{c_{Max}}$)

Voltages	Average voltage [V]	$\Delta V_{c_{Max}}$ [V]
$\hat{v}_{c_1}$	12.4	2.8
v_{c_1}	12.5	7.3
$\hat{v}_{c_2}$	25.0	2.6
v_{c_2}	25.1	5.8
$\hat{v}_{c_3}$	37.7	3.3
v_{c_3}	37.9	5.8
$\hat{v}_{c_4}$	50.3	3.9
v_{c_4}	50.6	6.3
$\hat{v}_{c_5}$	62.5	4.2
v_{c_5}	62.9	5.8
$\hat{v}_{c_6}$	75.5	3.9
v_{c_6}	76.0	6.3
$\hat{v}_{c_7}$	88.3	4.8
v_{c_7}	88.9	7.3
$\hat{v}_{c_8}$	100.5	4.3
v_{c_8}	101.4	6.3

Equation (21), which means that the estimated values are accurate. Moreover, considering the measurement noise, the voltage ripples are in concordance with Equation (20), which defines the maximum voltage ripple in the capacitors.

The results presented in this section show that the estimation scheme tolerates uncertainties in the capacitance values. Indeed, the small errors introduced by the uncertainties are corrected at each sampling period, which prevents the errors from accumulating, as would happen in an open-loop scheme.

7.5 | Assessment of the computational burden

The computational burden account for the number of arithmetic or logic operations needed to implement the estimation algorithm. In this sense, the proposed algorithm requires about 48 sum operations and 42 multiplications to estimate eight voltages. We could say that for n estimates the number of additions and multiplications is given approximately by $(6 \times n)$ operations,

which is a low computational burden. Moreover, in terms of execution time the computational burden is determined by the processor speed.

8 | CONCLUSION

In this paper, an estimation scheme for the capacitor voltages in FCMC is introduced and experimentally tested in a 9-level laboratory prototype. The scheme is based on a system of $n + 1$ linear equations where the unknowns are the capacitor voltages. The first equation models the output voltage measurement as a linear combination of the actual capacitor voltages; the following n equations hold the information of the open-loop estimates. This approach allows estimating the capacitor voltages and input voltage at each sampling time. Indeed, the approximate solution of the system gives the best estimates of the voltages in the sense of least-squares-errors. Also, the solution is unique because the design matrix always has full column rank. Additionally, because the design matrix is sparse, it is possible to have explicit equations for each estimate. The resulting equations are simple, without any adjustable parameter. The only system parameter needed for the estimation is the capacitance value, but its impact in the estimate precision is low.

Furthermore, the estimation scheme was incorporated into a closed-loop control to regulate the output current and the capacitor voltages—the estimates of the capacitor voltages are used by the current regulation controller and by the capacitor voltages balance strategy. The obtained results confirm the excellent performance of the estimation scheme under different operating conditions (i.e. transient state, steady-state, and uncertain capacitance values). The obtained results show that the estimates can be used instead of direct measurements, saving the cost and design efforts, simplifying the hardware system, which is very attractive when the number of levels is high.

Finally, its simplicity and low computational burden make feasible its use in multilevel converters with a large number of capacitors. It allows using only one voltage sensor instead of n physical sensors, which is especially attractive when the number of required levels is high.

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